



of MOS transistors of a relatively matched size, wherein the matched pairs of MOS transistors are coupled to separate current mirrors that are arranged with complementary MOS transistors that have a relatively matched size.

5. (Original) The apparatus of Claim 1, wherein the detection circuit further includes a logic circuit that employs at least three voltages to band the position of the inflection point, wherein the at least three voltages are generated by at least three leakage currents in at least two pairs of MOS transistors of a relatively matched size, wherein the matched pairs of MOS transistors are coupled to separate current mirrors that are arranged with complementary MOS transistors that have a relatively matched size.

6. (Original) The apparatus of Claim 1, wherein the detection circuit further includes at least two pairs of MOS transistors of a relatively matched size, wherein the matched pairs of the MOS transistors are sized substantially larger than a minimum size for the plurality of MOS transistors, and wherein the substantially larger size of the matched MOS transistors enables the initial leakage current to be detectable by the detection circuit.

7. (Cancelled)

8. (Original) The apparatus of Claim 1, wherein the back bias voltage is coupled to a substrate shared by the bulk terminals for the plurality of MOS transistors.

9. (Original) The apparatus of Claim 1, wherein the back bias voltage is a reverse bias voltage applied to a bulk terminal of the plurality of MOS transistors.

10. (Original) The apparatus of Claim 1, further comprising a battery that supplies power to the integrated circuit, wherein the reduction in the value of the leakage current causes a decrease in the amount of power drawn in an idle state by the integrated circuit from the battery.



